Semiconductor memory chip module

This invention relates to a semiconductor memory chip module having a plurality of memory chips of different types, in particular a plurality of memory chips executed in different production technologies. In particular, the invention relates to a semiconductor memory chip module suitable for smart cards and to a smart card equipped with such a chip module.

Currently available semiconductor memories can be assigned to different types in accordance with their production technology, their operating parameters, their capacitance, etc. Semiconductor memories can for example be divided into volatile and nonvolatile memories.

In smart cards and smart card terminals it is expedient to use nonvolatile memories whose content can also be erased and overwritten. Typically used semiconductor memories for such purposes are EEPROMs.

Such EEPROMs, i.e. erasable, electrically programmable read-only memories, necessitate some circuit complexity for erasing and rewriting data and require relatively long access time in comparison to volatile memories, for example a DRAM or SRAM. If such a semiconductor memory is used during execution of software programs, only slow execution is possible for the program. In addition, an EEPROM permits only a limited number of erase and write operations, typically in the range of 10,000 to 100,000.

If the presence of a nonvolatile memory, for example an EEPROM, is required but a rapid-access memory is nevertheless desired for program execution, one idea is to provide in addition to the EEPROM for example a SRAM as a volatile memory which is then used for program execution. If the results are to be stored for some time after execution of a program, the required data can be reloaded to the EEPROM.

The different types of semiconductor memories, that is, in the present case nonvolatile memories (EEPROMs) and rapid volatile memories (SRAMs), are based on different production technologies. If two such different types of semiconductor memories are used side by side, considerable effort is required for operationally interconnecting the two memories. Relatively long conduction paths are necessary between the two memories. This takes up a relatively large portion of the available chip area.

DE 196 26 337 A1 describes the simultaneous use of chips with volatile and nonvolatile memories for storing data. EP 0 328 062 A2 at the same time starts out from use in a smart card, so that EP 0 328 062 A2 has the features of the preamble of the independent claims. However, neither document indicates anything about the geometric structure or arrangement of the chips.

US 5,840,417 describes in general the vertical arrangement and contacting of electronic chips, whereas US 5,229,647 describes the vertical arrangement and contacting of memory chips of the same type. Neither document deals with the problems resulting from the use of different types of memory chips.

The invention is based on the problem of providing a semiconductor memory chip module which permits the advantages of two types of memory chips without the stated disadvantages, that is, high production effort and long conduction paths.

This problem is solved by the features of claim 1. According to the invention, a semiconductor memory chip module with different types of memory chips is formed in that the memory chips are disposed one above the other in different levels and connected by vertical interconnections.

In an especially preferred embodiment, there is a fixed allocation of memory cells of the first memory chip to memory cells of the second memory chip, the mutually allocated memory cells being directly interconnected by the vertical connections.

In an especially preferred embodiment, the first type of memory chip is a nonvolatile memory, in particular EEPROM, and the second type a volatile memory, for example a SRAM.

The invention allows production of a semiconductor memory chip module having different types of memory chips, in particular memory chips fabricated by different production technologies. The chips can according to the invention be produced separately, with the aid of the production processes typical of them. The finished chips require relatively little chip area in each case. The finished chips are then stacked, the connections between the chips being vertical connections, i.e. requiring very little additional chip area. The chip stack is then formed as a self-contained unit, in particular packaged into one module, so that it can be mounted in a smart card.

In the simplest embodiment of the invention, two chip levels can be provided. Since each semiconductor memory includes not only the actual memory cells but also a drive circuit, referred to as a decoder here, said decoders can be formed together with the particular semiconductor chip. In an especially advantageous embodiment of the invention, however, it is provided that a further chip with decoder circuits for all memory chips of the chip module is provided in a further level. The chip occupying area is thus not increased - in the horizontal direction - by the decoder circuits in the further chip. The chip with the decoder circuits is also connected by vertical chip interconnections to the memory chip of the first or second type, depending on which chip is located directly under the chip with the decoder circuits.

A special feature in using memory chips in connection with smart cards and smart card terminals is the protection from so-called power analysis attacks. In such attacks an attempt is made with fraudulent intent to analyze current and voltage states on a circuit with the aid of special sensors in order to be able to infer protected data. If voltage and current levels which always assume one, or one of several, defined levels independently of internal circuit states are ensured on all connections, such an attack is impossible.

A constantly recharged capacitor, a so-called buffer capacitor, can be used to smooth the supply voltage for the chip to such an extent that no level changes are outwardly recognizable which could permit circuit states to be inferred.

In a preferred embodiment of the invention it is provided that an energy buffer, in particular in the form of an integrated capacitor, is formed in at least one of the levels of the chip module. Said buffer capacitor can occupy a total chip level, but in a preferred multilayer design it can also be limited only to a partial chip area so that the rest of this level is available for memory cells, decoder circuits or logic circuits. Said buffer capacitor can be used, at the end of processing of a program performed with the aid of the volatile memory, to store the results of the program and further data in the nonvolatile memory. In case of a program abortion caused by external disturbing influences for example, the data necessary for restarting the program can be stored permanently in the nonvolatile memory with the aid of the buffer capacitor.

In the following, some examples of the invention will be explained in more detail with reference to the drawing, in which:

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Figure 1 shows a schematic vertical sectional view of a semiconductor memory chip module according to a first embodiment of the invention; and

Figure 2 shows a view similar to Figure 1 of a second embodiment of the invention.

Figure 1 shows semiconductor memory chip module 2 according to a first embodiment of the invention. Chip module 2 contains three stacked chips, namely bottom chip 4, formed here as an EEPROM, i.e. a nonvolatile memory chip, middle chip 6, formed here as an SRAM, i.e. a volatile memory chip, and top chip 8 comprising two types of decoder circuits 10 and 12.

Memory chip 4 contains a predetermined number of memory cells C4. Aligned therewith in the vertical direction, memory chip 6 contains a corresponding number of volatile memory cells C6.

Memory cells C4 and C6 in memory chips 4 and 6 are vertically aligned, as indicated by vertical lines in Figure 1. Between mutually vertically allocated memory cells C4 and C6 there is a direct electric connection through so-called vertical chip interconnections, to be explained in more detail below for the example shown in Figure 2.

Decoder circuits 10 and 12 contained in the top level in top chip 8 permit different addressing capabilities for memory chips 4 and 6. In the present embodiment, decoder circuits 10 (only one being shown in Figure 1) serve to drive memory cells C4 in bottom memory chip 4 while decoder circuits 12 serve to drive memory cells C6 in middle memory chip 6. In a modified embodiment, however, decoder circuits 10 and 12 can also be used for both memory chips 4 and 6 in each case.

Figure 2 shows a second embodiment of semiconductor memory chip module 2' which is structured on the basis of the chip module shown in Figure 1.

As in the first embodiment, bottom chip 4 is formed as an EEPROM, in the next level above is chip 6 formed as an SRAM. Mutually vertically aligned memory cells C4 and C6 are directly connected electrically by vertical chip interconnections 16.

Similar vertical chip interconnections connect memory chip 6 with chip 8, which contains decoder circuits (not shown in detail) and additionally buffer capacitor 20. Buffer capacitor 20 is likewise connected by direct vertical chip interconnections 22a with memory chip 6 located below and by chip interconnections 22b with further chip

16 located above, and is furthermore connected by a connection indicated at 24 with the decoder circuits contained in chip 8. Through connections not shown also connect buffer capacitor 20 with bottom memory chip 4.

Semiconductor memory chip module 2' of the embodiment shown in Figure 2 contains not only buffer capacitor 20, which acts as an energy buffer, but also chip 16 in an uppermost level, said chip containing for example logic circuits whose function is available for all other chips 4, 6 and 8.

In the embodiment according to Figure 2, buffer capacitor 20 is produced from a plurality of alternating electroconductive and dielectric layers. A feeder (not shown) is used to hold buffer capacitor 20 constantly at a supply voltage level. Its capacitance is such that it allows data to be written from the SRAM of memory chip 6 to corresponding memory cells of the EEPROM of memory chip 4 in the case of service abortion of chip module 2' for example.

The invention and the embodiments of a chip module shown in Figures 1 and 2 are suitable in particular for incorporation in a smart card or smart card terminal, albeit the invention is not limited thereto. As a further modification of the invention, the order of the memory chips can be altered. In Figure 1 various chips 4, 6 and 8 can have their order changed for example. The same holds for the arrangement according to Figure 2. Buffer capacitor 20 can also extend over a total chip level. The decoder circuits, shown at 10 and 12 in top chip 8 in Figure 1, can also be distributed over different chip levels.

The examples of semiconductor memory chip modules shown in Figures 1 and 2 contain chips 4, 6, 8 and 16 fabricated in separate production processes. The separately fabricated chips are stacked and vertically interconnected by bonding. Bonding refers in this case to connecting the individual chips or wafers containing chips. For this purpose the chips or wafers can be thinned, i.e. their thickness reduced after production. The actual electric interconnection of the individual chips or wafers is effected by vertical chip interconnections, as described above. The vertical chip interconnections are produced by a metalization process corresponding to the metalization process during production of the individual chips or wafers. This permits a high connection density, which e.g. allows individual memory cells to be interconnected electrically in different levels, i.e. on different chips, as described above. This moreover causes an increase in

above. This moreover causes an increase in security since the internal vertical chip interconnections are not accessible from outside and thus cannot be tapped for analysis purposes.

The thus obtained total arrangement is encased and then available for mounting in a smart card for example. Encasing including the outwardly guided interconnecting leads will not be explained in detail here because it is conventional.

When mounted in a smart card the semiconductor memory chip module according to Figure 1 or Figure 2 works in such a way that the permanently stored data are located in bottom chip 4, that is, in the nonvolatile memory EEPROM. Upon execution of programs, required data are reloaded to the middle chip, that is, the volatile memory (SRAM). Middle chip 6 then acts like a cache memory. Result data and data to be protected in case of service abortion for example are then reloaded from middle memory chip 6 to bottom memory chip 4, using the energy stored in the buffer capacitor.